**Review of Lesson Plan – Digital System Design (EC303PC)**

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| **Faculty Name:** Y. Vishwa Sri | Year / Sem: II/I | Academic Year: 2020-21 |

W.e.f. 18-Octoberber-2021

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| **L. No** | **Name of the Topic** | **Plan Date** | **Actual Date** | **Remarks** |
| 1 | **Unit 1: Number system and Boolean Algebra and switching Functions,** Introduction to subject | 18-10-21 |  |  |
| 2 | Introduction Binary Numbers | 19-10-21 |  |  |
| 3 | Number Systems | 20-10-21 |  |  |
| 4 | Number Conversions: Binary to hexadecimal, Hexadecimal to binary, Binary to Octal, Octal to Binary Conversion |  |  |  |
| 5 | Octal to Hexadecimal, Hexadecimal to Octal Conversion, Decimal to any Radix, Any Radix to decimal |  |  |  |
| 6 | Complements of Numbers |  |  |  |
| 7 | Binary Arithmetic using Complements (TBS) |  |  |  |
| 8 | Binary Codes, BCD codes |  |  |  |
| 9 | Excess-3, Gray code |  |  |  |
| 10 | Error Detecting and Correcting Codes, Parity bit, Hamming code |  |  |  |
| 11 | Boolean Algebra and Laws of Boolean algebra |  |  |  |
| 12 | Basic theorems |  |  |  |
| 13 | Switching Functions |  |  |  |
| 14 | Digital Logic Gates, Properties of XOR Gates |  |  |  |
| 15 | Universal Gates |  |  |  |
| 16 | Multilevel NAND/NOR realizations |  |  |  |
| 17 | **Unit-II: Minimization and Design of Combinational Circuits, :** Introduction, The Minimization of switching function using theorem |  |  |  |
| 18 | The Karnaugh Map Method-Up to three Variable Maps |  |  |  |
| 19 | The Karnaugh Map Method-Four and Five Variable Maps |  |  |  |
| 20 | Example problems on k-map |  |  |  |
| 21 | Don’t care conditions |  |  |  |
| 22 | Tabular Method |  |  |  |
| 23 | Combinational logic design: Introduction, Analysis procedure |  |  |  |
| 24 | Adders: Half adder, Full adder |  |  |  |
| 25 | Binary adder, Carry look ahead adder, BCD adder, Excess-3 adder, Serial adder (TBS) |  |  |  |
| 26 | Subtractor: Half subtractor, Full Subtractor, Binary subtractor |  |  |  |
| 27 | Magnitude Comparator |  |  |  |
| 28 | Decoders, Encoders |  |  |  |
| 29 | Multiplexers, Demultiplexers |  |  |  |
| 30 | Code Converters, Hazards and Hazard free realization |  |  |  |
| 31 | **Unit-III: Sequential Machines Fundamentals and Applications: Introduction,** Distinctions between Combinational and Sequential, The Binary Cell, Fundamentals of Sequential Machine Operation circuits |  |  |  |
| 32 | Latches |  |  |  |
|  | **I Mid Examination** |  | | |
| 33 | Flip Flops: SR, JK, Race Around Condition in JK |  |  |  |
| 34 | D and T Type Flip Flops |  |  |  |
| 35 | JK Master Slave Flip Flop |  |  |  |
| 36 | Excitation Table of all Flip Flops |  |  |  |
| 37 | Design of a Clocked Flip-Flop |  |  |  |
| 38 | Timing and Triggering consideration, Clock Skew |  |  |  |
| 39 | Conversion from one type of Flip-Flop to another |  |  |  |
| 40 | Conversion from one type of Flip-Flop to another |  |  |  |
| 41 | Shift Registers, Data Transmission in Shift Registers |  |  |  |
| 42 | Operation of Shift Registers, Shift Register Configuration |  |  |  |
| 43 | Bidirectional Shift Registers, Applications of Shift Registers |  |  |  |
| 44 | Design and Operation of Ring and Twisted Ring Counter |  |  |  |
| 45 | Operation Of Asynchronous Counters |  |  |  |
| 46 | Operation Of Synchronous Counters |  |  |  |
| 47 | **Unit IV: Sequential Circuits – I,** Introduction, State Diagram |  |  |  |
| 48 | Analysis of Synchronous Sequential Circuits |  |  |  |
| 49 | Approaches to the Design of Synchronous Sequential Finite State Machines |  |  |  |
| 50 | Synthesis of Synchronous Sequential Circuits |  |  |  |
| 51 | Serial Binary Adder |  |  |  |
| 52 | Sequence Detector |  |  |  |
| 53 | Parity-bit Generator |  |  |  |
| 54 | Design of Asynchronous Counters |  |  |  |
| 55 | Design of Asynchronous Counters |  |  |  |
| 56 | Design of Synchronous Modulo N – Counters |  |  |  |
| 57 | Design of Synchronous Modulo N – Counters |  |  |  |
| 58 | **Unit V: Sequential Circuits – II,** Finite state machine-capabilities and limitations |  |  |  |
| 59 | Mealy model |  |  |  |
| 60 | Moore model |  |  |  |
| 61 | minimization of completely specified sequential machines |  |  |  |
| 62 | minimization of incompletely specified sequential machines |  |  |  |
| 63 | Partition techniques |  |  |  |
| 64 | Partition techniques |  |  |  |
| 65 | Merger chart methods |  |  |  |
| 66 | Merger chart methods |  |  |  |
| 67 | concept of minimal cover table |  |  |  |
| 68 | Revision |  |  |  |
|  | **Mid-2 Examination** |  | | |

**TEXT BOOKS**:

**T1:** Digital Design-M Morris Mano, PHI, 5th Edition.

**T2:** Computer System Architecture, M. Morris Mano, 3rd Edition, Pearson

**REFERENCE BOOKS:**

**R1**: Switching and Finite Automata Theory, Z Kohavi, Tata McGraw Hill

**R2:** Fundamentals of Logic Design, C.H Roth, L l Kinney, 7th edition, Cengage learning

**R3:** Fundamentals of digital logic & micro computer design, 5th edition, M.Rafiquzzamman, John Wiley

**ADDITIONAL BOOKS:**

**A1:** Switching theory and logic design-A Anand kumar,PHI

**A2:** Digital Logic design- A.P Godse, Dr D A Godse, Technical Publications

**Web References:**

**W1:** nptel.ac.in/courses/106102062/16

**W2:** nptel.ac.in/courses/117105080/3

**W3:** nptel.ac.in/courses/117103064/21

**W4:** nptel.ac.in/courses/117106086/11

**W5:** nptel.ac.in/courses/117106086/30

**W6:** nptel.ac.in/courses/122104013/node32.html

**W7:** nptel.ac.in/courses/117101058/downloads/Lec-30.pdf

**W8:** nptel.ac.in/courses/117106092/4

**W9:**nptel.ac.in/reviewed\_pdfs/106102062/lec28.pdf

**Signature of faculty Signature of HOD**